ELEC 3004/7312: Signals Systems & Controls
PRACTICAL LABORATORY ONE REPORT
Due: 20th April, 2012

Note: This practical laboratory report is worth **5%** of the final course mark (it is worth 50% of the Practical 1 and Practical 2 Assignment, which together is worth 10% of the course mark). You should spend approximately 3 hours preparing for the report. The tutors will *not* assist you further unless there is real evidence you have attempted questions prior to the tutorial. Beyond the lecture and tutorial sessions, it is estimated that you will need 4 to 5 hours to complete the assignment (**7-8 hours total**). Remember that this should be turned in via the submission system.

Total marks: 100

1. **[20] Pre-lab**

   Before the laboratory started, there were seven questions to answer (repeated below for clarity). Please submit answers to these.

   1. Tabulate the two's complement binary representation of the decimal numbers -8 to 7. How many bits are required to do this? Identify the "sign bit" and the most significant bit.
   2. Tabulate the unsigned binary representation of the decimal numbers 0 to 15. If this binary representation is then "shifted" (i.e., AC coupled) so that 0 represents –VDD/2 and 15 represents +VDD/2, again, identify the "sign bit" and the most significant bit.
   3. Given the PMOD-AD1 can handle a range of input levels from GND to VDD (where VDD = 5v) and it has a 12-bit, unipolar binary analogue to digital (ADC), what is the quantisation step-size of the ADC?
   4. The PMOD-DA2 is a 12-bit unipolar DAC with an output range from GND to VDD (where VDD = 5v). What is the quantisation step-size of its output?
   5. Can you explain how the code in SINEWAVE.VHD generates a sine wave? Can you predict the effect of increasing the number of samples in the LUT?
   6. For 12-bit unsigned binary, what are the maximum and minimum decimal values?
   7. Convert the minimum and maximum values, as well as 2048, 2831 and 3495 to hexadecimal, then into 12-bit binary. What are the values of I (index) for these values in the Look-up-table in the appendix?

2. **[40] Laboratory Part 1**

   In Part 1 of the Laboratory Procedure, there are five questions about the device's operation. They are repeated for clarity. Please answer them briefly.

   1. Plot the output waveform/s on the oscilloscope. What is the amplitude and frequency of the sine wave generated on each available channel?
   2. The Master Clock is 50MHz, which is then divided by 200, in clockdiv1.vhd, to produce Fr. This frequency, Fr, controls the readout rate of the LUT which is n=16 elements long. If it takes 16 clock cycles of Fr to produce a complete LUT cycle, what is the theoretical audio output frequency? Is it the same as your measured frequency?
   3. Can you derive the simple equation for the audio output frequency, based on the value of clockdiv1,and n = the length of the LUT?
   4. Try to confirm that the DAC step size is approximately the same as that calculated in the preparation. If it is not, can you explain why?
   5. Suggest how you might modify the VHDL code so that a LUT with only 8 points is required. What are the advantages and disadvantages of this approach?

3. **[10] Laboratory Part 2**

   In Part 2 of the Laboratory Procedure, there are three questions about the device's operation. Please answer the last one. It is repeated for clarity.

   What would you need to do to generate a sine wave of an arbitrary frequency? Can you write some Matlab code that generates the values required for the LUT?

Continued on Page 2 …

4. **[15] Laboratory Part 3**

   In Part 3, Step 8 of the Laboratory Procedure, there are three questions about the device's operation. Please answer the first three. They are repeated for clarity.

   1. What amplitude and frequency do you observe on each channel?
   2. How could you halve the amplitude?
   3. How could you double or halve the frequency?

5. **[15] Overall System Review**

   Looking at the overall laboratory, ***what are the limitation(s) on the process of digitizing a signal? How might they be overcome when designing a system?***

   Hint: *Be sure to consider the entire process from the Nexys2 Board and its connectors, to the sampling frequency, to the quantization of the signal*