ELEC3004/7312: Signals Systems & Controls

EXPERIMENT 1: INTRODUCTION TO THE NEXYS 2

Aims

In this laboratory session you will:

1. Gain familiarity with the workings of the **Digilent Nexys 2** for DSP applications;
2. Have a first look at the **Xilinx ISE** software for FPGA programming, using both VHDL and schematics, as well as **Digilent Adept** download software;
3. Appreciate the use of a look-up-table (**LUT**) method for generating periodic signals, such as sine waves.
4. See the effects of reconstruction filters.

Introduction

Preparation

Note: (Individual) Preparation will be checked and marked at the start of each laboratory class. Hand in your preparation answers on a sheet to your tutor before the lab session. Keep a copy to work with in the lab. Preserve your marked sheet once returned. No preparation = no labs (no assessment). It will be best if you can maintain a log book for the labs.

Read and familiarise yourself with the following documents available from the course (or manufacturer's) website:

- The Nexys 2 Reference Manual Pages 1-5, 15; http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,789&Prod=NEXYS2
- Digilent PMOD interface boards: http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9
- PMOD DA2 Dual 12-bit DAC http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,401,487&Prod=PMOD-DA2
- PMOD AD1 Dual 12-bit ADC http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,401,499&Prod=PMOD-AD1

Answer the following questions:

1. Tabulate the two's complement binary representation of the decimal numbers -8 to 7. How many bits are required to do this? Identify the "sign bit" and the most significant bit.

2. Tabulate the unsigned binary representation of the decimal numbers 0 to 15. If this binary representation is then "shifted" (i.e., AC coupled) so that 0 represents $-V_{DD}/2$ and 15 represents $+V_{DD}/2$, again, identify the "sign bit" and the most significant bit.

3. Given the PMOD-AD1 can handle a range of input levels from GND to V_{DD} (where V_{DD} = 5v) and it has a 12-bit, unipolar binary analogue to digital (ADC), what is the quantisation step-size of the ADC?

4. The PMOD-DA2 is a 12-bit unipolar DAC with an output range from GND to VDD (where V_{DD} = 5v). What is the quantisation step-size of its output?

5. Can you explain how the code in SINEWAVE.VHD generates a sine wave? Can you predict the effects of increasing the number of samples in the LUT?

6. For 12-bit unsigned binary, what are the maximum and minimum decimal values?

7. Convert the minimum and maximum values, as well as 2048, 2831 and 3495 to hexadecimal, then into 12-bit binary. What are the values of I (index) for these values in the Look-up-table in the appendix?

Appendix:

Sinewave.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity SINEWAVE is port
   (
        DATAOUT      : out  std_logic_vector(11 downto 0);
        SAMPLECLK    : in   std_logic
   );
end SINEWAVE;


architecture behavioral of SINEWAVE is

signal I : integer range 0 to 15;

begin
            with I select
         DATAOUT <= "100000000000" when 0,     --800
                    "101100001111" when 1,     --B0F
                    "110110100111" when 2,
                    "111101100011" when 3,
                    "111111111111" when 4,
                    "111101100011" when 5,
                    "110110100111" when 6,
                    "101100001111" when 7,
                    "100000000000" when 8,
                    "010011110000" when 9,
                    "001001011000" when 10,
                    "000010011100" when 11,
                    "000000000000" when 12,
                    "000010011100" when 13,
                    "001001011000" when 14,
                    "010011110000" when 15;

            I <= I + 1 when rising_edge(SAMPLECLK);
   end behavioral;
```